In the claims:

Claims 1 - 8 (Canceled).

9. (Previously presented) An edge seal around the periphery of an integrated circuit device comprising:

a semiconductor substrate;

a layer of low-k dielectric material over the semiconductor substrate;

a layer of hard material over or under the layer of low-k dielectric material, the layer of hard material selected from the group consisting of a dielectric material and a hard mask material; and

an edge seal structure around the periphery of an integrated circuit device comprising:

a metallic wall of a high conductivity metal in the layer of low-k dielectric material and in the layer of hard material; and

a layer of insulation material on sidewalls of the metallic wall between the metallic wall and the low-k dielectric material and between the metallic wall and the layer of hard material, wherein the insulation material and low-k dielectric material are different materials and wherein the insulation material is selected from the group consisting of SiO_2, SiC, Si_3N4, Al_2O_3, diamond like carbon, polyimide and combinations thereof.

10. (Original) The edge seal of claim 9 wherein the low-k dielectric material comprises SiLK or fluoridized polyimide.

11. (Previously presented) The edge seal of claim 9 wherein the layer of hard material comprises a bottom layer on the semiconductor substrate under the low-k dielectric material and a top moisture barrier on the low-k dielectric material.

Claim12. (Canceled)

13. (Original) The edge seal of claim 9 further comprising a barrier layer between the metallic wall and the insulation material wherein the barrier layer is selected from the group consisting of tantalum, tantalum nitride, chromium/ chromium oxide, titanium, titanium nitride, tungsten silicide and combinations thereof.

14. (Original) The edge seal of claim 9 wherein the high conductivity metal is copper.

15. (Original) The edge seal of claim 9 wherein the thickness of the insulation material is 0.05 microns to 0.5 microns.

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16. (Previously presented) An edge seal around the periphery of an integrated circuit device comprising:

a semiconductor substrate;

a layer of dielectric material over the semiconductor substrate, the layer of dielectric material comprising a low-k dielectric material; and

an edge seal structure around the periphery of an integrated circuit device comprising:

a metallic wall of a high conductivity metal in the layer of dielectric material, wherein the metallic wall comprises spaced-apart via-studs physically connected by an interconnection line; and

a layer of insulation material between the metallic wall and the dielectric material, wherein the insulation material and dielectric material are different materials, and wherein the layer of insulation material is between the dielectric material and each of the via-studs.

Claim 17 (Canceled).

18. (Currently amended) An edge seal around the periphery of an integrated circuit device comprising:

a semiconductor substrate;

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a layer of dielectric material over the semiconductor substrate, the layer of dielectric material comprising a low-k dielectric material; and

an edge seal structure around the periphery of an integrated circuit device comprising:

a metallic wall comprising two spaced-apart via studs physically connected by an interconnection line in the layer of dielectric material, the via studs having a length; and

a wall of insulation material extending the full length of the via studs and between the metallic wall and the periphery of the integrated circuit device, wherein the insulation material and dielectric material are different materials.